Amendments to the Specification:

Please replace the paragraph beginning at page 3, line 17, with the following amended paragraph:

First, in the period T1, a sampling pulse, LAT is input from a shift register. Then, the LAT is at [[H]] L level ~~(5V)~~ (-2V) while the LATB is at [[L]] H level ~~(-2V)~~ (5V) , thereby turning ON the P-channel TFT 2001 and the N-channel 2004. At this time, when the DATA is at H level (3V), the P-channel TFT 2002 is turned OFF while the N-channel TFT 2003 is turned ON. Thus, the clocked inverter 2005 outputs VSS. At this time, however, if the threshold voltage $|V_{TH}|$ of the P-channel TFT 2002 is 2 V or less, the P-channel TFT 2002 is incidentally turned ON and thus a leakage current flows.

Please replace the paragraph beginning at page 14, line 1, with the following amended paragraph:

The timing chart in this embodiment is similar to the timing chart of Embodiment Mode 1 shown in FIG. 1(B). Therefore, description is given here with reference to FIG. 1(B). First, in the reset period T1, the LAT-1 is at H level (5 V), whereby the first reference switch 7003, the second reference switch 7004 and the switch ~~7008~~ 7007 for setting the threshold value are turned ON. Then, the node a is at a potential of DH (3 V) while the node a' is at a potential of DL (0 V). The node b is at the threshold voltage (assumed to be 2 V here) of the correction inverter 7008.

Please replace the paragraph beginning at page 14, line 16, with the following amended paragraph:

As described above, according to the data latch circuit of this embodiment mode, an accurate operation can be obtained without being influenced by the TFT characteristics even when the amplitude of an input signal is small ~~relatively~~ relative to the width of a power supply voltage. Therefore, low power consumption and high frequency operation can be achieved. Furthermore, according to the data latch circuit of this embodiment mode, by setting one of the

two reference potentials, which are input to the two reference switches respectively, at the highest potential (DH) of the data signal while setting the other at the lowest potential ([[~~DH~~]]DL) of the data signal, an intermediate potential used for the reference potential is not particularly required, which contributes to the reduction in the number of power supplies.

Please replace the paragraph beginning at page 16, line 26, with the following amended paragraph:

As described above, according to the data latch circuit of this embodiment mode, an accurate operation can be obtained without being influenced by variations in the TFT characteristics even when the amplitude of an input signal is smaller than those of other Embodiment modes, ~~relatively~~ relative to the width of a power supply voltage. Therefore, low power consumption and high frequency operation are achieved. Furthermore, according to the data latch circuit of this embodiment mode, by setting one of the two reference potentials, which are input to the two reference switches respectively, at the highest potential (DH) of the data signal while setting the other at the lowest potential ([[~~DH~~]]DL) of the data signal, an intermediate potential used for the reference potential is not particularly required, which contributes to the reduction in the number of power supplies.